Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **J**
2. **D**
3. **C**
4. **B**
5. **A**
6. **N/C**
7. **VSS**
8. **N/C**
9. **E**
10. **F**
11. **G**
12. **H**
13. **K**
14. **VDD**

**.061”**

**.061”**

**2 1 14 13**

**3**

**4**

**5**

**7 9**

**12**

**11**

**10**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask Ref: 10093**

**APPROVED BY: DK DIE SIZE .061” X .061” DATE: 2/14/17**

**MFG: HARRIS THICKNESS .020” P/N: CD4082B**

**DG 10.1.2**

#### Rev B, 7/1